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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,178	12/02/2003	Simon Robert Walmsley	PEA09US	4574

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EXAMINER	
DOAN, DUC T	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/727,178	WALMSLEY, SIMON ROBERT	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-6 are in the application.

Claims 1-6 are rejected.

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in AUSTRALIA on 12/02/02. It is noted, however, that applicant has not filed a certified copy of the 2002953134 2002953135 applications as required by 35 U.S.C. 119(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6 rejected under 35 U.S.C. 103(a) as being anticipated by Mehrotra et al (US 6145054).

As for claim 1, Mehrotra describes a method of updating a cache in an integrated circuit comprising: the cache (Fig 1: #105 cache; column 1 lines 60-68) a processor connected to the cache via a cache bus (Fig 1: #102, processor connecting with the cache #105; column 1 lines 60-68); a memory interface (Fig 4) connected to the cache via a first bus (Fig 1: #107, main memory and #105 cache) and to the processor via a second bus (Fig 1: #102), the first bus being wider than the second bus or the cache bus (Mehrotra's Fig 6B, column 13 lines 62 to column 14 lines 15 describes the cache using the read port 8 bytes wide to supply data back to the processor, and using fill port 32 bytes wide for data returning from memory) ; and memory connected to the memory interface via a memory bus (Fig 4: #107); the method comprising the steps of:

(a) following a cache miss, using the processor to issue a request for first data via a first address, the first data being that associated with the cache miss (Mehrota's column 9 lines 1-10);

(b) in response to the request, using the memory interface to fetch the first data from the memory, and sending the first data to the processor (Mehrotra's column 9, lines 21-30, level 1 generate a cache access request to level 2);

(c) sending, from the memory interface and via the first bus, the first data and additional data, the additional data being that stored in the memory adjacent the first data (Mehrotra's column 9 lines 1-5, cache fill operation);

(d) updating the cache with the first data and the additional data via the first bus (Mehrotra's column 9 lines 21-25 passing returned data to lower cache levels); and

(e) updating flags in the cache associated with the first data and the additional data, such that the updated first data and additional data in the cache is valid (Mehrotra's column 9 lines 8-12, valid cache line status bit).

As for claim 2, the claim recites wherein the processor is configured to attempt a cache update with the first data upon receiving it from the memory interface, the method further including the step of preventing the attempted cache update by the processor from being successful, thereby preventing interference with the cache update of steps (d) and/or (e). Mehrotra's column 13 lines 33-50 describes a read miss/write miss situation in which the subsequence write operation is not completed until previous read data is returned in the cache.

As for claim 3, the claim recites method according to claim 2, wherein steps (c), (d), and (e) are performed substantially simultaneously (Mehrotra's column 3 lines 1-27 describe the non-blocking cache architectures in which multiples steps and multiple requests are processed concurrently).

As for claim 4, the claim recites wherein steps (d) and (e) are performed by the memory interface. Mehrotra's column 13 lines 53-55 describes each cache level has entities which can generate access requests to the cache.

As for claim 5, the claim recites wherein steps (d) and (e) are performed in response to the processor attempting to update the cache following step (c). Mehrotra's column 13 lines 38-50 describes handling the write miss including generating a read miss to the next higher cache level, and the requested data is then returned and written into the cache.

As for claim 6, the claim recites wherein the memory interface is configured to monitor the processor to determine when it attempts to update the cache following step (c). Mehrotra's column 13 lines 31-35 describes each cache level is provided with a buffer to store the data associated with the write request until the write hit is achieved.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 1/6/06

DD

Mano Padmanabhan

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER

Supervisory Patent Examiner

TC2100